

|                                   |  |                         |   |             |
|-----------------------------------|--|-------------------------|---|-------------|
| <b>Notice of References Cited</b> |  | Application/Control No. | Applicant(s)/Patent Under Reexamination |             |
|                                   |  | 10/699,910              | SEWARD, ROBERT YOUNG                    |             |
| Examiner                          |  | Art Unit                |   | Page 1 of 2 |
| Phallaka Kik                      |  | 2825                    |   |             |

**U.S. PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name               | Classification |
|---|---|--|-----------------|--------------------|----------------|
| * | A | US-5,784,289 A                                   | 07-1998         | Wang, Deborah Chao | 716/8          |
| * | B | US-5,784,600 A                                   | 07-1998         | Doreswamy et al.   | 713/503        |
| * | C | US-5,880,969 A                                   | 03-1999         | Hama et al.        | 716/12         |
| * | D | US-6,154,874 A                                   | 11-2000         | Scepanovic et al.  | 716/13         |
| * | E | US-6,219,823 B1                                  | 04-2001         | Hama et al.        | 716/12         |
| * | F | US-2001/0018759 A1                               | 08-2001         | ANDREEV et al.     | 716/7          |
| * | G | US-6,687,892 B1                                  | 02-2004         | Zahar, Sharon      | 716/12         |
| * | H | US-6,792,585 B1                                  | 09-2004         | Ku et al.          | 716/10         |
| * | I | US-6,886,149 B1                                  | 04-2005         | Teig et al.        | 716/12         |
| * | J | US-2006/0010412 A1                               | 01-2006         | Teig et al.        | 716/008        |
| * | K | US-2006/0206848 A1                               | 09-2006         | Teig et al.        | 716/010        |
|   | L | US-  |                 |                    |                |
|   | M | US-  |                 |                    |                |

**FOREIGN PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | Classification |
|---|---|--|-----------------|---------|------|----------------|
|   | N |  |                 |         |      |                |
|   | O |  |                 |         |      |                |
|   | P |  |                 |         |      |                |
|   | Q |  |                 |         |      |                |
|   | R |  |                 |         |      |                |
|   | S |  |                 |         |      |                |
|   | T |  |                 |         |      |                |

**NON-PATENT DOCUMENTS**

|   |   |   |
|---|---|---|
| * |   | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)   |
|   | U | Caldwell et al., "On Wirelength Estimations for Row-Based Placement", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, No. 9, September 1999, pp. 1265-1278.     |
|   | V | Jeong et al., "Finding Optimal Module Orientations in Macrocell Placement", Electronics Letters, Vol. 27, No. 10, 9 May 1991, pp. 804-805.  |
|   | W | Zhong et al., "Effective Partition-Driven Placement with Simultaneous Level Processing and Global Net Views", IEEE/ACM International Conference on Computer-Aided Design, 5 November 2000, pp. 254-259. |
|   | X | Jackson et al., "Estimating and Optimizing RC Interconnect Delay During Physical Design", IEEE International Symposium on Circuits and Systems, 1-3 May 1990, vol. 2, pp. 869-871.                      |

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

|                                   |                          |   |             |
|-----------------------------------|--------------------------|---|-------------|
| <b>Notice of References Cited</b> | Application/Control No.  | Applicant(s)/Patent Under Reexamination |             |
|                                   | 10/699,910               | SEWARD, ROBERT YOUNG                    |             |
|                                   | Examiner<br>Phallaka Kik | Art Unit<br>2825                        | Page 2 of 2 |

**U.S. PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name | Classification |
|---|---|--|-----------------|------|----------------|
|   | A | US-  |                 |      |                |
|   | B | US-  |                 |      |                |
|   | C | US-  |                 |      |                |
|   | D | US-  |                 |      |                |
|   | E | US-  |                 |      |                |
|   | F | US-  |                 |      |                |
|   | G | US-  |                 |      |                |
|   | H | US-  |                 |      |                |
|   | I | US-  |                 |      |                |
|   | J | US-  |                 |      |                |
|   | K | US-  |                 |      |                |
|   | L | US-  |                 |      |                |
|   | M | US-  |                 |      |                |

**FOREIGN PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | Classification |
|---|---|--|-----------------|---------|------|----------------|
|   | N |  |                 |         |      |                |
|   | O |  |                 |         |      |                |
|   | P |  |                 |         |      |                |
|   | Q |  |                 |         |      |                |
|   | R |  |                 |         |      |                |
|   | S |  |                 |         |      |                |
|   | T |  |                 |         |      |                |

**NON-PATENT DOCUMENTS**

| * |   | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)  |
|---|---|--|
|   | U | Yang et al., "Circuit Clustering for Delay Minimization Under Area and Pin Constraints", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 9, September 1997, pp. 976-986. |
|   | V |  |
|   | W |  |
|   | X |  |

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.